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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,452	01/02/2001	Tomoyoshi Kushida	P 275517 TJ9701US-C1	7172

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,452	KUSHIDA, TOMOYOSHI	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings corrections were received on 11/25/2003, and are approved by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Akiyama et al. (5,182,626).

Regarding claim 1, Akiyama et al. teach in figure 11 and related text (column 12, lines 17-44) an IGBT device comprising: a FET switching element 6 provided on a surface of a semiconductor layer 2; a substrate 1 at another surface of the semiconductor layer; a portion of the semiconductor layer located between the switching element and the substrate having an impurity concentration sufficient enough so that a region adjacent to the substrate is not depleted; a defect region 2A provided in a portion of the semiconductor layer includes an entire non depletion layer, wherein the non-depletion layer is not depleted after a switch-off operation; and a half-valued width of a lattice

defect concentration of the defect region is thicker than the thickness of the non-depletion layer, a peak of lattice defect concentration within the non-depletion layer (see figure 12), wherein the lattice defect concentration in the non-depletion layer is sufficient to shorten lifetime of carriers and reduce turn-off time; and a switching control G (gate) having a current flowing in a thickness direction of the semiconductor layer when the switching element is turned on and off.

Although Akiyama et al. do not explicitly disclose a defect region concentration is sufficient to shorten lifetime of carriers and reduce turn-off time, this feature is inherent in Akiyama et al.'s device, because defect regions serve as recombination centers for holes which reduce the hole current, shorten lifetime of carriers and thus reduce the turn-off time of the device.

Although Akiyama et al. do not explicitly disclose a portion of the semiconductor layer located between the switching element and the substrate having an impurity concentration sufficient enough so that a region adjacent to the substrate is not depleted, wherein the entire non depletion layer is included within the defect region and not being depleted after a switch off operation, these features are inherent in Akiyama et al.'s device for the following reasons. Akiyama et al. teach a defect region being formed within the high concentration N+ region 2A, adjacent to a low concentration N- region 2B. During switch off operation, the gate electrode is biased such that electrons and holes in the low concentration region 2B are recombined and distinguished. A depletion layer is formed in the low concentration region, resulting in turning off the device. Since recombination in the low concentration region results in turning off the

device, the entire high concentration region 2A remains non-depleted after a switch off operation, and thus a portion of the semiconductor layer located between the switching element and the substrate having an impurity concentration sufficient enough so that a region adjacent to the substrate is not depleted, as claimed.

Furthermore, regarding the claimed limitation of a defect region provided in a portion of the semiconductor layer includes an entire non depletion layer, the broad recitation of the claim dos not specify when a defect region includes an entire non depletion layer. Certainly during operation the defect region 2A includes an entire non-depletion layer. Therefore, Akiyama et al. teach a defect region 2A provided in a portion of the semiconductor layer includes an entire non-depletion layer, as claimed.

Regarding the claimed limitation of a half-valued width of a lattice defect concentration of the defect region being thicker than the thickness of the non-depletion layer, the thickness of defect region 2A is the thickness of the corresponding half-valued width of a lattice defect concentration. Defect region 2A includes the entire non-depletion layer therein. Therefore, the thickness of the half-valued width of a lattice defect concentration of the defect region is thicker than the thickness of the non-depletion layer, as claimed.

Regarding claim 2, Akiyama et al. teach in figure 11 a defect region 2A does not include the switching element 6.

Regarding claim 3, although Akiyama et al. do not explicitly disclose the life times of carriers in defect region 2A are shorter than those in other portions, this feature is inherent in Akiyama et al.=s device, because defect regions serve as recombination centers for holes which reduce the hole current, and thus shorten the lifetime of carriers therein.

Regarding claims 4 and 5, Akiyama et al. teach in figure 11 ad related text a bipolar transistor with an emitter 3, a base 2 and a collector 1 thereof laid out in the thickness direction of the semiconductor layer, wherein the switching element is a field-effect transistor which is turned on for injecting carriers to the base of the bipolar transistor.

Regarding claims 6 and 7, Akiyama et al. teach in figure 11 ad related text a defect region 2A includes an entire portion in the base 2 in close proximity to the emitter 3, which is not depleted after a switch-of f operation.

Regarding claims 8-11, Akiyama et al. teach in figure 11 ad related text the bipolar transistor and the field-effect transistor constitute an insulated-gate bipolar transistor (IGBT).

Response to Arguments

Applicant argues that Akiyama does not teach or suggest that a half-valued width of a lattice defect concentration of the defect region is thicker than the thickness of the

non-depletion layer, as recited in claim 1, because the defect distribution peak half-value width W is smaller than the width of layer 2A.

Although the defect distribution peak of the half-value width W is smaller than the width of layer 2A, crystal defects are distributed throughout the entire width of layer 2A. Since the thickness of defect region 2A is the thickness of the corresponding half-valued width of a lattice defect concentration, then defect region 2A includes the entire non-depletion layer therein. Therefore, Akiyama teaches the thickness of the half-valued width of a lattice defect concentration of the defect region is thicker than the thickness of the non-depletion layer.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers relat d to this application may be submitted to T chnology cent r (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via th TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
2/11/04

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800